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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,250	11/10/2003	William M. Hiatt	2269-5558A US (99-0253.00)	3203
24247	7590	06/15/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			SHECHTMAN, SEAN P	
			ART UNIT	PAPER NUMBER

2125

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/705,250

Applicant(s)

HIATT ET AL.

Examiner

Sean P. Shechtman

Art Unit

2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/7/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 are presented for examination. Claims 1, 4, 8, 12, 16, 20, 24, and 31 have been amended.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following features must be shown or the feature(s) canceled from the claim(s). The substrate handling system comprising of a linear feed system (claims 3 and 14). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. Objections withdrawn due to the amendment.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 24-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 24 recites the limitation "the second fabrication site" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 3,889,355 to Aronsatein.

Referring to claims 1, 12, and 15, Aronsatein teaches a programmable material consolidation system (Col. 16, lines 1-68), comprising: at least one fabrication site for fabricating one or more objects using a programmed material consolidation process (Col. 26, lines 14-19; Col. 6, lines 3-49; Col. 11, lines 10-44); and a substrate handling system configured to introduce one or more substrates into the at least one fabrication site and remove the one or more substrates from the fabrication site (Col. 26, lines 14-36).

Referring to claims 2 and 13, Aronsatein teaches the programmable material consolidation system of claim 1, wherein the substrate handling system comprises a rotary feed system (Col. 9, lines 1-14).

Referring to claims 3 and 14, Aronsatein teaches the programmable material consolidation system of claim 1, wherein the substrate handling system comprises a linear feed system (Col. 26, lines 14-36).

Referring to claims 4 and 16, Aronsatein teaches the programmable material consolidation system of claim 1, wherein the at least one fabrication site comprises a plurality of fabrication sites (Col. 26, lines 14-36).

Referring to claims 5 and 17, Aronsatein teaches the programmable material consolidation system of claim 4, wherein the substrate handling system is configured to introduce the one or more substrates into each of the plurality of fabrication sites (Col. 26, lines 14-36).

Referring to claims 6 and 18, Aronsatein teaches the programmable material consolidation system of claim 1, further comprising: a cleaning component for cleaning the one or more substrates (Col. 8, lines 65-68).

Referring to claims 7 and 19, Aronsatein teaches the programmable material consolidation system of claim 6, wherein the substrate handling system is configured to transport the one or more substrates having at least one feature fabricated thereon from the at least one fabrication site to the cleaning component (Col. 8, lines 65-68).

Referring to claims 8 and 20, Aronsatein teaches the programmable material consolidation system of claim 7, wherein the at least one fabrication site comprises a plurality of fabrication sites (Col. 11, lines 59-68; Col. 18, lines 61-68).

Referring to claims 9 and 21, Aronsatein teaches the programmable material consolidation system of claim 8, wherein the substrate handling system is configured to transport

substrates from each of the plurality of fabrication sites to the cleaning component (Col. 11, lines 59-68).

Referring to claims 10 and 22, Aronsatein teaches the programmable material consolidation system of claim 9, further comprising: at least one processing element for controlling operation of the substrate handling system (Col. 24, lines 17-41).

Referring to claims 11 and 23, Aronsatein teaches the programmable material consolidation system of claim 10, wherein the at least one processing element is configured to orchestrate movement of substrates from the plurality of fabrication sites to the cleaning component (Col. 24, lines 17-41).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 24-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 4,027,246 to Caccoma in view of U.S. Pat. No. 3,889,355 to Aronsatein.

Referring to claims 24, Caccoma teaches a programmed material consolidation method for fabricating objects (Col. 8, lines 25-34), comprising: selecting at least one first substrate; introducing the at least one first substrate into a first fabrication site with a substrate handling system associated therewith; selecting at least one second substrate; and introducing the at least one second substrate into a second fabrication site with the substrate handling system (See Abstract).

Referring to claim 25, Caccoma teaches the method of claim 24, wherein introducing the at least one second substrate is effected while one or more objects are being fabricated on the at least one first substrate (Col. 11, lines 51-55).

Referring to claim 26, Caccoma teaches the method of claim 24, further comprising: selecting at least one third substrate; and introducing the at least one third substrate into a third fabrication site with the substrate handling system (Col. 11, lines 62- Col. 12, line 4).

Referring to claim 27, Caccoma teaches the method of claim 26, wherein introducing the at least one third substrate is effected while one or more objects are being fabricated on both the at least one first substrate and the at least one second substrate (Col. 11, lines 51-55).

Referring to claim 28, Caccoma teaches the method of claim 24, further comprising: removing the at least one first substrate from the first fabrication site with the substrate handling system while one or more objects are being fabricated on the at least one second substrate (Col. 11, lines 51-55).

Referring to claim 24, Caccoma teaches all the limitations set forth above, and Caccoma clearly cross references the semiconductor wafer processing sectors of Aronsatein several times, for example, in column 7, lines 13-15 and column 8, lines 25-34. However, Caccoma fails to clearly teach that semiconductor wafer processing sectors of Aronsatein fabricate at least a portion of at least one object by a programmed material consolidation process. The examiner respectfully submits that the claims, as such, do not even require that the portion of the object fabricated, the object, or the fabricating be related to any substrates selected or introduced.

Referring to claims 29 and 32, Caccoma teaches all the limitations set forth above, however, fails to clearly teach transporting the a substrate to a cleaning component with the

Art Unit: 2125

substrate handling system following removing of the substrate. Referring to claims 30 and 33, Caccoma teaches all the limitations set forth above, however, fails to clearly teach introducing another substrate into a fabrication site with the substrate handling system following removing of a substrate. Referring to claim 31, Caccoma teaches all the limitations set forth above, however, fails to clearly teach removing a substrate from a fabrication site with the substrate handling system while an object is being fabricated on both the substrate and another substrate.

However, referring to claim 24, the Aronsatein reference that is cross referenced by the Caccoma reference and shares a common assignee with Caccoma, teaches analogous art, wherein the same semiconductor wafer processing sectors referenced by Caccoma fabricate at least a portion of at least one object by a programmed material consolidation process (Col. 26, lines 14-19; Col. 6, lines 3-49; Col. 11, lines 10-44). Referring to claims 29 and 32, Aronsatein teaches transporting the a substrate to a cleaning component with the substrate handling system following removing of the substrate (Col. 8, lines 65-68); referring to claims 30 and 33, Aronsatein teaches introducing another substrate into a fabrication site with the substrate handling system following removing of a substrate (Col. 24, lines 17-41); and referring to claim 31, Aronsatein teaches removing a substrate from a fabrication site with the substrate handling system while an object is being fabricated on other substrates (Col. 9, lines 14-49; Col. 10, lines 35-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Caccoma with the teachings of Aronsatein, who's patent is cross referenced several times in Caccoma. One of ordinary skill in the art would

have been motivated to combine these references because Aronsatein teaches a complete manufacturing system capable of fast turn-around, maximized yield and low in-process inventory with interdependent minimization of processing cycle time and maximization of completed part yield (Col. 1, lines 4-19). Furthermore, Aronsatein clearly teaches “parts of the photolithographic operations are distributed throughout the line in a manner designed to maximize yield and minimize control complexity” (Col. 6, lines 46-49). Further still, Aronsatein clearly teaches “Each of the sectors is also envisioned to be under suitable control, either by general purpose computer or a hard-wired system, to specify and maintain process parameters, and to maintain proper flow of work-pieces for the sector.” (Col. 3, lines 42-47).

Response to Arguments

Applicant's arguments filed April 28th 2005 have been fully considered but they are not persuasive.

7. Applicant argues that Figs. 1 and 2 clearly show a rotary feed system. Applicant further argues that, in view of 37 C.F.R. 1.83 (a), the detailed illustration of a linear feed system is not essential for proper understanding of the invention.

In response, the examiner respectfully invites applicant's attention to 37 C.F.R. 1.83 (a) which clearly states:

§ 1.83 Content of drawing.

- (a) The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).

Clearly every feature of the invention specified in the claims must be shown as stated in the previous office action, at the very least "in the form of a graphical drawing symbol or labeled representation".

Should applicant argue that the feed system shown is a conventional feature shown by a graphical drawing symbol or labeled representation (although, it appears that applicant has stated that the feed system explicitly shown in the drawings is the clearly the rotary feed system), the examiner would object to the drawings under 37 CFR 1.84(h)(5) because both Figures 1 and 2 show(s) modified forms of construction in the same view.

8. Applicant argues that Aronsatein does not teach fabrication sites for effecting or using a programmed material consolidation system. The examiner respectfully disagrees. For applicant's convenience the examiner has provided a portion of the instant specification below, wherein applicant describes the programmed material consolidation system:

"The present invention includes stereolithography apparatus and other programmable material consolidation apparatus and systems that are configured to fabricate features on semiconductor devices or on components that are configured for use with semiconductor devices. In addition, the present invention includes stereolithographic and other programmed material consolidation methods (e.g., stereolithography, layered object manufacturing (LOM), selective laser sintering (SLS), photopolymer jetting, selective particle atomization and consolidation (laser engineered net shaping, or "LENS"), and other so-called "rapid prototyping" technologies) that include use of apparatus according to the present invention. As used herein, the term "stereolithography" and variations thereof, where applicable, are intended to denote all types of programmed material consolidation techniques and is used synonymously with the phrase "programmed material consolidation" and variations thereof." (See Page 5, paragraph 14).

Aronsatein clearly teaches sectors are performing semiconductor processing "photolithographic operations" on a wafer (Col. 6, lines 3-49). The examiner respectfully submits that, at the very least, semiconductor processing "photolithographic operations" on a wafer meet applicants broad definition of other programmed material consolidation methods.

The examiner also respectfully submits that it is inherent that semiconductor processing “photolithographic operations” on a wafer is “layered object manufacturing”. *Although not relied upon in claims rejected under Aronsatein* the examiner notes column 1, lines 23-57 of U.S. Pat. No. 5,455,894 to Conboy, which clearly states, in part:

“The fabrication of a semiconductor wafer is well known. Fabrication often begins by the patterning of a particular sequence of successive layers upon the wafer. Patterning of layers, often called photolithography, involves many steps. The first step might be to create silicon dioxide insulating layer on the surface of the silicon wafer. Thereafter, removal of selective portions or sections of the insulting layer may be achieved to expose underlying silicon. Selective removal of silicon dioxide is achieved by spinning a photoresist material across the silicon dioxide surface. A mask is used to allow a source of ionizing radiation to impinge at selective locations across the wafer. Depending upon whether the photoresist is positive-type or negative-type photoresist, certain areas of photoresist may dissolve when exposed to solvents thereby exposing selective areas of silicon dioxide. Thereafter, the exposed portions of silicon dioxide can be removed by etching techniques commonly known in the art.”

Photolithography is the patterning of sequence of successive layers upon the wafer and it is well known in the art.

Furthermore, not only is it inherent that photolithography is the patterning of sequence of successive layers upon the wafer, Aronsatein clearly teaches layered object manufacturing. In column 6, lines 40-42, Aronsatein clearly teaches in sector 1A “growth of an oxide on the wafer, and the application of a layer of photoresist material over the oxide coating”. In column 11, lines 10-44, Aronsatein clearly teaches in sector 1C “During the residence of the wafers passage through the oxidation furnace 74 and after having the oxide layer built up to a desired thickness, the wafers will be subjected to an appropriate dopant, such as a phosphorous oxide chloride (POCl₃) gas for appropriate modification of the oxide layer.”

The examiner submits that, although Aronsatein does not say the words “programmed material consolidation”, Aronsatein does meet this claim limitations in more ways than one.

9. Applicant argues that Aronsatein does not teach a substrate handling system that comprises a rotary feed system. The examiner respectfully disagrees.

Applicant admits that Aronsatein teaches a handler may rotate wafers from a horizontal position to a vertical position. Applicant appears to argue that said rotation is linear. The examiner is unable to determine how applicant can interpret said rotation as being linear. The examiner respectfully submits that said rotation is rotary.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

11. The prior art or art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents or publications are cited to further show the state of the art with respect to photolithography

U.S. Pat. No. 5,455,894 to Conboy.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean P. Shechtman whose telephone number is (571) 272-3754. The examiner can normally be reached on 9:30am-6:00pm, M-F.

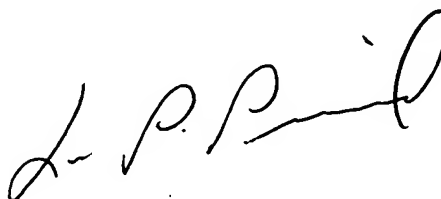
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SPS

Sean P. Shechtman

June 8, 2005

A handwritten signature in black ink, appearing to read 'L. P. Picard', with a stylized flourish at the end.

**LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100**